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EXAMINER	
TSAI, HENRY	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/927,625	Applicant(s) CISMAS, SORIN C.	
	Examiner Henry W.H. Tsai	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *8/9/01* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-5,7,8 and 19* is/are allowed.

6)☒ Claim(s) *6, 9-11, and 16-18* is/are rejected.

7)☒ Claim(s) *12-15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. Claims 10-15, and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 10, line 30, "the first input token"; and line 34 "the first input context token" lack proper antecedent basis since they were not defined previously.

In claim 17, line 31, "the first output token"; and lines 32-33 "the first input token" lack proper antecedent basis since they were not defined previously.

Applicant is required to review the claims and correct all language which does not comply with 35 U.S.C. § 112, second paragraph.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 6, 9-11, and 16-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Faget et al. (U.S. Patent No. 5,907,691) hereafter referred to as Faget et al.'691.

Referring to claim 6, Faget et al.'691 discloses as claimed a data-flow and context-flow data processing system, comprising a plurality of data-driven cores (204, 224, and 244 see Fig. 4), each of the cores including: a) a context identification storage unit (260, see Fig. 6, see also col. 18, lines 24-32, regarding input register 260 receives incoming information packet and their associated type data) for storing a current context identification token (the TYPE field see TABLE I comprising such as bits 0 and 3 for identifying "snuff" Read/Write or "buff" Read/Write inside the TYPE filed see TABLE I); and b) logic (interface logic see Fig. 6) for controlling a flow of the current context identification token (the TYPE filed see TABLE I

comprising such as bits 0 and 3 for identifying "unbuff" Read/Write or "buff" Read/Write inside the TYPE filed see TABLE I) through the cores (204, 224, and 244 see Fig. 4) such that the current context identification token (the TYPE filed see TABLE I comprising such as bits 0 and 3 for identifying "unbuff" Read/Write or "buff" Read/Write inside the TYPE filed see TABLE I) is transferred from a first core (204 see Fig. 4) to a second core (224 see Fig. 4) upon a synchronous assertion of a request signal (B RDY or U RDY signals, see Fig. 4 are best reasonably and broadly interpreted as the input request signal since they provide the same feature as claimed) from the second core (224 see Fig. 4) to the first core (204 see Fig. 4), and of a ready signal (the signal of "Valid" bit <8> inside the TYPE field see TABLE I for indicating the validity of each of the portions of an information packet. See Col. 17, lines 55-65 regarding "if the Valid bit is a '0', bits <7:0> of the type field are ignored. Additionally, Bit <3> of the type field typically is used to identify whether a buffered (i.e., non-priority) information path or an unbuffered (i.e., priority) information path should be used to: (1) transfer information from the interface circuit to the core processor, (2) transfer information from the core processor to the interface circuit, or

(3) hold information in the backup information path") from the first core (204 see Fig. 4) to the second core (224 see Fig. 4).

Referring to claim 9, Faget et al.'691 discloses as claimed a data- and context-flow data processing system comprising a plurality of cores (204, 224, and 244 see Fig. 4), each of the cores comprising: a) an input control bus (the bus on the left hand side of the interfaces 206, 226, and 246 for CLK, B RDY, U RDY, BUSY, see Fig. 4) for transferring input control signals (the signals of CLK, B RDY, U RDY, BUSY on the left hand side of the interfaces 206, 226, and 246, see Fig. 4); b) an input token bus for receiving input tokens in response to assertions of the input control signals, the input tokens including an input data token (INFO on the left hand side of the interfaces 206, 226, and 246 see Fig. 4 and see also TABLE II) to be processed by the core, and an input context identification token (the TYPE field on the left hand side of the interfaces 206, 226, and 246 see also TABLE I comprising such as bits 0 and 3 for identifying "unbuff" Read/Write or "buff" Read/Write inside the TYPE filed see TABLE I) for specifying a current context; c) an output control bus (the bus on the right hand side of the interfaces 206, 226, and 246 for CLK, B RDY, U RDY, BUSY, see Fig. 4) for transferring output control signals (the signals on the right hand side of the interfaces 206, 226, and 246 for CLK, B RDY, U

RDY, BUSY, see Fig. 4); and d) an output token bus (the bus of type and info on the right hand side of interface 226 see Fig. 4) for sending output tokens in response to assertions of the output control signals, the output tokens including an output data token (INFO on the right hand side of the interfaces 206, 226, and 246 see Fig. 4 and see also TABLE II) derived from the input data token (INFO on the left hand side of the interfaces 206, 226, and 246 see Fig. 4 and see also TABLE II), and an output context identification token (the TYPE field on the right hand side of the interfaces 206, 226, and 246 see also TABLE I comprising such as bits 0 and 3 for identifying "unbuff" Read/Write or "buff" Read/Write inside the TYPE filed see TABLE I) equal to (note inherently this is one possible situation) the input context identification token (the TYPE field on the left hand side of the interfaces 206, 226, and 246 see also TABLE I comprising such as bits 0 and 3 for identifying "unbuff" Read/Write or "buff" Read/Write inside the TYPE filed see TABLE I), for specifying the current context.

Referring to claim 10, Faget et al.'691 discloses as claimed a multithreaded data processing system comprising a first data-driven core (224 see Fig. 4), a second data-driven core (204 see Fig. 4), and a third data-driven core (244 see Fig. 4) integrated on a chip, the first core comprising: a) a

first input interface (interface 226, see Fig. 4) connected to the second core (204 see Fig. 4), comprising a first input request connection for asserting a first input request signal (B RDY or U RDY signals one the left hand side of interface 226, see Fig. 4 are best reasonably and broadly interpreted as the input request signal since they provide the same feature as claimed) to the second core (204 see Fig. 4), a first input ready connection for receiving a first input ready signal (the signal of "Valid" bit <8> inside the TYPE field one the left hand side of interface 226, see also TABLE I for indicating the validity of each of the portions of an information packet. See Col. 17, lines 55-65 regarding "if the Valid bit is a '0', bits <7:0> of the type field are ignored. Additionally, Bit <3> of the type field typically is used to identify whether a buffered (i.e., non-priority) information path or an unbuffered (i.e., priority) information path should be used to: (1) transfer information from the interface circuit to the core processor, (2) transfer information from the core processor to the interface circuit, or (3) hold information in the backup information path") asserted by the second core (204 see Fig. 4), and a first input data connection for receiving from the second core (204 see Fig. 4) an input context token (the TYPE field on the left hand side of the interfaces 226 see also TABLE I

comprising such as bits 0 and 3 for identifying "unbuf" Read/Write or "buff" Read/Write inside the TYPE filed see TABLE I) for establishing a context state for the first core (224 see Fig. 4); b) processing logic connected to the first input interface, for processing a data token (INFO on the left hand side of the interfaces 226 see Fig. 4 and see also TABLE II) according to the context state; c) a first output interface (note interface 226 is also an output interface, see Fig. 4) connected to the third core, comprising a first output request connection for receiving a first output request signal (B RDY or U RDY signals one the right hand side of interface 226, see Fig. 4 are best reasonably and broadly interpreted as the input request signal since they provide the same feature as claimed) asserted by the third core, a first output ready connection for asserting a first output ready signal (the signal of "Valid" bit <8> inside the TYPE field one the right hand side of interface 226, see also TABLE I for indicating the validity of each of the portions of an information packet. See Col. 17, lines 55-65 regarding "if the Valid bit is a '0', bits <7:0> of the type field are ignored. Additionally, Bit <3> of the type field typically is used to identify whether a buffered (i.e., non-priority) information path or an unbuffered (i.e., priority) information path should be used to: (1) transfer information

from the interface circuit to the core processor, (2) transfer information from the core processor to the interface circuit, or (3) hold information in the backup information path") to the third core, and a first output data connection connected to the processing logic, for transmitting to the third core a first output context token (the TYPE field on the right hand side of the interfaces 226 see also TABLE I comprising such as bits 0 and 3 for identifying "unbuff" Read/Write or "buff" Read/Write inside the TYPE filed see TABLE I) derived from the first input token, for establishing the context state for the third core (244 see Fig. 4); d) first input control logic (the interface 226 logic see Fig. 6) connected to the first input interface, for controlling the first core (224 see Fig. 4) to receive the first input context token (the TYPE field on the left hand side of the interfaces 226 see also TABLE I comprising such as bits 0 and 3 for identifying "unbuff" Read/Write or "buff" Read/Write inside the TYPE filed see TABLE I) for establishing a context state for the first core (224 see Fig. 4) if the first input request signal and the first input ready signal are asserted with a predetermined synchronous relationship (note Faget et al.'691 is broadly and reasonably interpreted as having the predetermined synchronous relationship since the predetermined synchronous relationship can be different from the truly

synchronous relationship); and e) first output control logic connected to the first output interface (the interface 226 logic see Fig. 6), for controlling the first core (224 see Fig. 4) to transmit the first output context token (the TYPE field on the right hand side of the interfaces 226 see also TABLE I comprising such as bits 0 and 3 for identifying "unbuff" Read/Write or "buff" Read/Write inside the TYPE filed see TABLE I) to the third core (244 see Fig. 4) if the first output request signal and the first output ready signal are asserted with a predetermined synchronous relationship (as set forth above, Faget et al.'691 broadly and reasonably to be interpreted as having the predetermined synchronous relationship since the predetermined synchronous relationship can be different from the truly synchronous relationship).

As to claim 11, Faget et al.'691 also discloses: a) the first input control logic comprises logic for controlling the first core to receive the first input context token if the first input request signal and the first input ready signal are asserted synchronously (note certainly this is the "if" and "better" condition for the Faget et al.'691's system); and b) the first output control logic comprises logic for controlling the first core to transmit the first output context token to the third core if the first output request signal and the first

output ready signal are asserted synchronously (note certainly this is the "if" and "better" condition for the Faget et al.'691's system).

Referring to claim 16, Faget et al.'691 discloses as claimed a multithreaded data processing system comprising a first data-driven core (224, see Fig. 4) and a second data-driven core (204, see Fig. 4), the first core (224, see Fig. 4) comprising an input interface (interface 226 see Fig. 4) connected to the second core (204, see Fig. 4), the input interface (interface 226 see Fig. 4) including: a) an input request connection for asserting an input request signal (B RDY or U RDY signals, see Fig. 4 are best reasonably and broadly interpreted as the input request signal since they provide the same feature as claimed) to the second core (204, see Fig. 4); b) an input ready connection for receiving an input ready signal (the signal of "Valid" bit <8> inside the TYPE field see TABLE I for indicating the validity of each of the portions of an information packet. See Col. 17, lines 55-65 regarding "if the Valid bit is a '0', bits <7:0> of the type field are ignored. Additionally, Bit <3> of the type field typically is used to identify whether a buffered (i.e., non-priority) information path or an unbuffered (i.e., priority) information path should be used to: (1) transfer information from the

interface circuit to the core processor, (2) transfer information from the core processor to the interface circuit, or (3) hold information in the backup information path") asserted by the second core (204, see Fig. 4); and c) an input data connection (INFO bus see Fig. 4 and see also TABLE II) for receiving from the second core (204, see Fig. 4), upon a synchronous assertion (inherently existing in the Faget et al.'691's system) of the input request signal (B RDY or U RDY signals, see Fig. 4 are best reasonably and broadly interpreted as the input request signal since they provide the same feature as claimed) and the input ready signal("Valid" bit <8> inside the TYPE filed see TABLE I), a first input context identification token (such as bits 0 and 3 for identifying "unbuff" Read/Write or "buff" Read/Write inside the TYPE filed see TABLE I) identifying a current context state.

Referring to claim 17, Faget et al.'691 ,as best understood, discloses as claimed a multithreaded data processing system comprising a first data-driven core (224 see Fig. 4), a second data-driven core (204 see Fig. 4), and a third data-driven core (244 see Fig. 4) integrated on a chip, the first core(224 see Fig. 4) comprising: a) an input interface (206, see Fig. 4) connected to the second core (204 see Fig. 4), comprising a control bus (the bus on the left hand side of the

interfaces 226 for CLK, B RDY, U RDY, BUSY, see Fig. 4) for transmitting a set of first control signals (the signals of CLK, B RDY, U RDY, BUSY on the left hand side of the interfaces 226, see Fig. 4) between the first core (224 see Fig. 4) and the second core (204 see Fig. 4), and an input data bus for receiving from the second core (204 see Fig. 4), upon the assertion of the set of first control signals according to a predetermined protocol an input data token (INFO on the left hand side of the interfaces 226 see Fig. 4 and see also TABLE II), and an input context identification token (the TYPE field on the left hand side of the interfaces 226 see also TABLE I comprising such as bits 0 and 3 for identifying "unbuff" Read/Write or "buff" Read/Write inside the TYPE filed see TABLE I) for establishing a current context state in the first core; b) processing logic (the interface 226 logic as shown in Fig. 6) connected to the first input interface, for generating an output data token (INFO on the right hand side of the interface 226 see Fig. 4 and see also TABLE II) from the input data token (INFO on the left hand side of the interface 226 see Fig. 4 and see also TABLE II) according to the context state; and c) an output interface (note the interface 226 is also an output interface) connected to the third core (244 see Fig. 4), comprising an output control bus (the bus on the right hand side of the

interface 226 for CLK, B RDY, U RDY, BUSY, see Fig. 4) for transmitting a set of second control signals (the signals on the right hand side of the interface 226 for CLK, B RDY, U RDY, BUSY, see Fig. 4) between the first core (224 see Fig. 4) and the third core (244 see Fig. 4), and an output data bus (the bus of type and info on the right hand side of interface 226 see Fig. 4) connected to the processing logic, for transmitting to the third core (244 see Fig. 4), upon the assertion of the set of first control signals (the signals of CLK, B RDY, U RDY, BUSY on the left hand side of the interfaces 226, see Fig. 4) according to the predetermined protocol the first output token, and a first output context token (the TYPE field on the right hand side of the interfaces 226 see also TABLE I comprising such as bits 0 and 3 for identifying "unbuff" Read/Write or "buff" Read/Write inside the TYPE filed see TABLE I) derived from the first input token, for establishing the current context state in the third core (244 see Fig. 4).

Referring to claim 18, Faget et al.'691 discloses as claimed a data- and context-flow data processing method comprising the steps of: a) establishing a first data- and context-driven core (204 see Fig. 4) and a second data- and context-driven core (224 see Fig. 4), the second core (224 see Fig. 4) being connected to the first core (204 see Fig. 4) for

receiving data tokens (INFO see Fig. 4 and see also TABLE II) and context tokens (the TYPE filed see TABLE I comprising such as bits 0 and 3 for identifying "unbuff" Read/Write or "buff" Read/Write inside the TYPE filed see TABLE I) from the first core (204 see Fig. 4); and b) operating the first core (204 see Fig. 4) in a first context (TYPE from core 244 interface 246 to core 204 interface 206 see Fig. 4), and concurrently (see Col. 17, line 27), operating the second core (224 see Fig. 4) in a second context (TYPE from core 204 interface 206 to interface 226 see Fig. 4) different from the first context.

Allowable Subject Matter

4. Claims 12-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. Claims 1-5, 7, 8, and 19 are allowed.

6. The following is a statement of reasons for the indication of allowable subject matter: Faget et al.'691, the closest

reference, and the other prior art do not teach or fairly suggest:

each core comprising a plurality of distributed multi-context storage units comprising: a context register bank; a context identification register; and logic for processing a set of data tokens according to the current context parameter set. (in claims 1, and 5);

the step of: retrieving a set of context parameters corresponding to the current context from each of a plurality of multi-context storage units distributed through the cores (in clam 7);

the first core comprising: a context identification register connected to the input interface; a multi-context storage unit connected to the context identification register; and control and processing logic (in claim 8); and

the pipestages including a plurality of distributed multi-context storage units each storing a plurality of context parameters and each responsive to the context identification tokens (in claim 19) in combination with all of the other limitations of the respective independent claims and the combination is not obvious.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure wherein Mather, III et al.'989 discloses a coprocessor interface comprising the control bus (for such as ready and request signals) and data bus between the coprocessor and the main microprocessor; Stanis et al.'241 discloses an inventory control, bed allowance and accounting data handling system also comprising several control signals such as a RDY signal as the claimed invention.

Contact Information

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (703) 308-7600. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (703) 305-9712. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **TC 2100 receptionist whose telephone number is (703) 305-3900.**

9. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into **the Group at fax number:** 703-872-9306.

This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER

May 25, 2004